REMARKS/ARGUMENTS

Claims 1-27 are pending in the application; reexamination and reconsideration are hereby requested.

1. Claims 1-27 were rejected as indefinite. The Examiner cited items of claims 1, 11, 19, and 24-26 as not apparent in the preferred embodiments, plus queried the "proportional" in claim 2.

Applicant replies that claims 1 and 11 read on Fig.6 with the "input transistors" as Q3, Q5; the line 4 "circuit" as current mirror 38; the translinear circuit is "configured" to add current by M2 and the left I_X input both connect to the emitter of Q3 and thereby the Q3 emitter current is the sum of I_X and I_{M2} and also by M3 and the right I_X input both connect to the emitter of Q5 and thereby the Q5 emitter current is the sum of I_X and I_{M3}; the translinear circuit operation in a segment is when Q7 is turned on or turned off; and the singularity is when the inputs I_X are 0 which would (without circuit 38) turn off Q3 and Q5 to cause the singularity. but the singularity is removed by I_{M2} and I_{M3} which keep transistors Q3 and Q5 turned on. The "implementing" of claim 11 means "which provides" or "characterized by".

With regard to claim 2, the input currents are proportional to each other.

For claim 19 the "detecting" a region for a translinear circuit removable singularlity is finding where both the transfer function denominator and numerator have a zero (application page 11, lines 6-9) with regions defined by input current intervals where a set number of clamps are active (e.g., claim 20); "determining" the input currents are the I_xs in Fig.6 and application page 11, lines 6-9; the "defining" the substantially equal perturbation currents are the relative sizes of M1 and M2 in Fig.6 (application page 11, line 4); and the steps of the method are apparent from the operation of the corresponding items in Fig.6.

For claim 24 the "pair of translinear loops" (e.g., Figs.4-5) in Fig.6 are Q2-Q1-Q3-Q4 and Q2-Q1-Q5-Q6; the "current mirror" in Fig.6 is 38; and the "clamp transistor" in Fig.6 is Q7.

For claim 25 the “input transistors” in Fig.6 are Q3 and Q5; the “current mirror” in Fig.6 is 38; the “clamp transistor” in Fig.6 is Q7; and the “control transistor” in Fig.6 is M1.

For claim 26 the three “limb”s in Fig.6 are Q1-Q2, Q3-Q4, and Q5-Q6 (e.g., Fig.2); the “a voltage rail” on line 8 has been amended to “said voltage rail”; the “first to sixth transistors” in Fig.6 are Q2-Q1-Q4-Q3-Q6-Q5; the “current sources” in Fig.6 are I_A, I_B , and I_C; the “current mirror” in Fig.6 is 38; the “current output” in Fig.6 is node with I_Y; and the “clamp transistor” in Fig.6 is Q7.

2. Claims 1-27 were rejected as anticipated by application prior art Figs.2-3. The Examiner cited input transistors Q1, Q4 with input currents I_A, I_C, current mirror M1-M4, current source I_X, control transistor Q11, and perturbation current circuit (16, 18, 20) in Fig.2 or (24, 26) in Fig.3.

Applicant replies that for Fig.2 (Fig.3) to be a translinear circuit, the common base connections imply that the limbs are Q2-Q1, Q3-Q4, Q5-Q6, (plus Q7-Q8 for Fig.3), and that the input transistors are selected from Q2, Q3, Q5, (plus Q7 for Fig.3) due to the emitter current inputs, so Q4 is not an input transistor because its emitter connects to a voltage rail, and I_C is not an input current because it is a collector current instead of an emitter current for an input transistor; the circuit (16,18,20) in Fig.2 are the translinear circuit limbs and thus do not add perturbation currents because they accept the input currents, and the circuit (24,26) of Fig.3 are likewise limbs and do not provide added perturbation currents. Consequently, neither Fig.2 nor Fig.3 suggests any of the claims.

Respectfully submitted,

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